# GANPAT UNIVERSITY

## FACULTY OF ENGINEERING & TECHNOLOGY

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|---|---|---|---|---|---|
| Programme | Diploma Engineering | | Branch | INFORMATION TECHNOLOGY | |
| Semester | IV | | Version | 1.0.0.0 | |
| Effective from Academic Year | 2018-19 | | Effective for the batch Admitted in | June 2018 | |
| Subject code | 1CE2405 | Subject Name | COMPUTER SYSTEM ARCHITECTURE | | |

| Teaching scheme | | | | | | Examination scheme (Marks) | | | |
|---|---|---|---|---|---|---|---|---|---|
| (Per week) | Lecture(DT) | | Practical(Lab.) | | Total | | CE | SEE | Total |
| | L | TU | P | TW | | | | | |
| Credit | 3 | 0 | 0 | 0 | 3 | Theory | 40 | 60 | 100 |
| Hours | 3 | 0 | 0 | 0 | 3 | Practical | 00 | 00 | 00 |

| Pre-requisites: |
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| Fundamental knowledge of computers |

| Course Learning Outcomes: |
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| The course content should be taught and implemented with an aim to develop different skills leading to the achievement of the following competencies and course learning outcomes:<br>T1. To learn the data transfer and micro-operation in computer system<br>T2. To draw flowchart of instruction and interrupt cycle<br>T3. To understand computer instruction set<br>T4. To Identify various types of memory in computers.<br>T5. To interface CPU-IOP communication<br><br>The practical should be carried out in such a manner that students are able to acquire different learning out comes in cognitive, psychomotor and affective domain to demonstrate course learning outcomes. |

| Course Content | | | | |
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| Name of UNIT | Unit Content | Unit Learning Outcomes | Marks | Hrs |
| UNIT – 1<br><br>REGISTER TRANSFER AND MICRO-OPERATIONS | 1.1 Register Transfer<br>1.2 Bus Transfer<br>1.3 Memory Transfer<br>1.4 Arithmetic Micro-operations<br>1.5 Logic Micro-operations<br>1.6 Shift Micro-operations<br>1.7 Arithmetic Logic Shift Unit | 1a. Define symbols for register Transfer<br>1b. Understand Bus Transfer and Memory Transfer<br>1b. Identify different types of Micro-operations | 10 | 08 |
| UNIT – 2<br><br>COMPUTER INSTRUCTION FORMAT | 2.1 Computer Registers<br>2.2 Computer Instruction Formats<br>2.3 Timing and Control Unit<br>2.4 Instruction Cycle<br>2.5 Memory Reference Instructions<br>2.6 I/O Reference Instructions<br>2.7 Interrupt Cycle | 2a. State the role of registers<br>2b. Develop a control timing signals<br>2c. List Memory and Input-Output Instructions<br>2d. Draw flowchart of Instruction Cycle and Interrupt Cycle | 15 | 10 |

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| UNIT – 3<br><br>COMPUTER INSTRUCTION SET | 3.1 CPU Instruction Formats<br>3.2 Addressing Mode<br>3.3 Data Transfer Instructions<br>3.4 Arithmetic Instructions<br>3.5 Logic Instructions<br>3.6 Shift Instructions<br>3.7 Program Control Instructions<br>3.8 Subroutine Call and Return | 3a. Interpret instruction format<br>3b. Classify types of instructions<br>3c. Understand operation of instruction set | 10 | 08 |
| UNIT – 4<br><br>MEMORY ORGANIZATION | 4.1 Memory Classifications<br>4.2 Main Memory<br>4.3 Memory Hierarchy<br>4.4 Auxiliary Memory<br>4.5 Associative Memory<br>4.6 Cache Memory<br>4.7 Virtual memory | 4a. Classify types of Memory<br>4b. Understand Memory Hierarchy<br>4c. Distinguish Auxiliary and Associative memory<br>4d. Describe Cache Mapping Scheme and Virtual map table | 15 | 10 |
| UNIT – 5<br><br>INPUT OUTPUT ORGANIZATION | 5.1 Input Output Interface Unit<br>5.2 Asynchronous Data Transfer<br>5.3 Asynchronous Serial Transfer<br>5.4 Input-Output Processor (IOP)<br>5.5 CPU-IOP Communication | 5a. Draw I/O Interface Unit<br>5b. List modes of data transfer<br>5c. Draw flowchart of CPU-IOP communication | 10 | 06 |

| List of Practical |
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| List of Instruments / Equipment / Trainer Board |
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| List of Reference Books | | | |
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| No | Title of Reference Books | Authors | Publication |
| 1 | Computer System Architecture | M. Morris Mano | Pearson |
| 2 | Computer Organisation and Architecture | Smruti Ranjan Sarangi | McGrawHill |
| 3 | Computer Architecture | Behrooz Parhami | Oxford |

| Link of Learning Web Resource | |
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| 1 | https://nptel.ac.in/courses/106103068/pdf/coa.pdf |
| 2 | https://lecturenotes.in/subject/9/computer-organisation-and-architecture-coa |
| 3 | https://lecturenotes.in/u/hiteshmomaya |