

GANPAT UNIVERSITY									
FACULTY OF ENGINEERING & TECHNOLOGY									
Programme	Diploma Engineering				Branch	Computer Engineering			
Semester	IV				Version	1.0.0.0			
Effective from Academic Year	2018-19				Effective for the batch Admitted in	June 2018			
Subject code	1CE2405		Subject Name	COMPUTER SYSTEM ARCHITECTURE					
Teaching scheme					Examination scheme (Marks)				
(Per week)	Lecture(DT)		Practical(Lab.)		Total		CE	SEE	Total
	L	TU	P	TW					
Credit	3	0	0	0	3	Theory	40	60	100
Hours	3	0	0	0	3	Practical	00	00	00

Pre-requisites:
Fundamental knowledge of computers

Course Learning Outcomes:
<p>The course content should be taught and implemented with an aim to develop different skills leading to the achievement of the following competencies and course learning outcomes:</p> <p>T1. To learn the data transfer and micro-operation in computer system</p> <p>T2. To draw flowchart of instruction and interrupt cycle</p> <p>T3. To understand computer instruction set</p> <p>T4. To Identify various types of memory in computers.</p> <p>T5. To interface CPU-IOP communication</p> <p>The practical should be carried out in such a manner that students are able to acquire different learning outcomes in cognitive, psychomotor and affective domain to demonstrate course learning outcomes.</p>

Course Content				
Name of UNIT	Unit Content	Unit Learning Outcomes	Marks	Hrs
UNIT – 1 REGISTER TRANSFER AND MICRO- OPERATIONS	1.1 Register Transfer 1.2 Bus Transfer 1.3 Memory Transfer 1.4 Arithmetic Micro-operations 1.5 Logic Micro-operations 1.6 Shift Micro-operations 1.7 Arithmetic Logic Shift Unit	1a. Define symbols for register Transfer 1b. Understand Bus Transfer and Memory Transfer 1b. Identify different types of Micro-operations	10	08
UNIT – 2 COMPUTER INSTRUCTION FORMAT	2.1 Computer Registers 2.2 Computer Instruction Formats 2.3 Timing and Control Unit 2.4 Instruction Cycle 2.5 Memory Reference Instructions 2.6 I/O Reference Instructions 2.7 Interrupt Cycle	2a. State the role of registers 2b. Develop a control timing signals 2c. List Memory and Input-Output Instructions 2d. Draw flowchart of Instruction Cycle and Interrupt Cycle	15	11

UNIT – 3 COMPUTER INSTRUCTION SET	3.1 CPU Instruction Formats 3.2 Addressing Mode 3.3 Data Transfer Instructions 3.4 Arithmetic Instructions 3.5 Logic Instructions 3.6 Shift Instructions 3.7 Program Control Instructions 3.8 Subroutine Call and Return	3a. Interpret instruction format 3b. Classify types of instructions 3c. Understand operation of instruction set	10	08
UNIT – 4 MEMORY ORGANIZATION	4.1 Memory Classifications 4.2 Main Memory 4.3 Memory Hierarchy 4.4 Auxiliary Memory 4.5 Associative Memory 4.6 Cache Memory 4.7 Virtual memory	4a. Classify types of Memory 4b. Understand Memory Hierarchy 4c. Distinguish Auxiliary and Associative memory 4d. Describe Cache Mapping Scheme and Virtual map table	15	10
UNIT – 5 INPUT OUTPUT ORGANIZATION	5.1 Input Output Interface Unit 5.2 Asynchronous Data Transfer 5.3 Asynchronous Serial Transfer 5.4 Input-Output Processor (IOP) 5.5 CPU-IOP Communication	5a. Draw I/O Interface Unit 5b. List modes of data transfer 5c. Draw flowchart of CPU-IOP communication	10	08

List of Practical

List of Instruments / Equipment / Trainer Board

List of Reference Books			
No	Title of Reference Books	Authors	Publication
1	Computer System Architecture	M. Morris Mano	Pearson
2	Computer Organisation and Architecture	Smruti Ranjan Sarangi	McGrawHill
3	Computer Architecture	Behrooz Parhami	Oxford

Link of Learning Web Resource	
1	https://nptel.ac.in/courses/106103068/pdf/coa.pdf
2	https://lecturenotes.in/subject/9/computer-organisation-and-architecture-coa
3	https://lecturenotes.in/u/hiteshmomaya